[29] Muslim, F. B., Ma, L., Roozmeh, M., & Lavagno, L. “Efficient FPGA implementation of OpenCL high-performance computing applications via high-level synthesis” *IEEE Access*, 5, 2747-2762, 2017.

[30] Sheng, Jiayi, et al. "Design of 3D FFTs with FPGA clusters." *2014* IEEE High-Performance Extreme Computing Conference *(HPEC)*.

[31] Sheng, Jiayi, et al. "HPC on FPGA clouds: 3D FFTs and implications for molecular dynamics." 2017 27th International Conference on Field Programmable Logic and Applications (FPL).

[32] Amendola, Roberto, et al. "APEnet+: a 3D Torus network optimized for GPU-based HPC Systems." *Journal of Physics: Conference Series*. Vol. 396. No. 4. IOP Publishing, 2012.

[33] Amendola, Roberto, et al. "Latest generation interconnect technologies in APEnet+ networking infrastructure." *Journal of Physics: Conference Series*. Vol. 898. No. 8. IOP Publishing, 2017.

[34] Joshi, Shubhangi M. "FFT architectures: a review." *International Journal of Computer Applications* 116.7 (2015).

[35] Ayinala, Manohar, Michael Brown, and Keshab K. Parhi. "Pipelined parallel FFT architectures via folding transformation." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 20.6 (2012): 1068-1081.

[36] Garrido, Mario, Keshab K. Parhi, and Jesús Grajal. "A pipelined FFT architecture for real-valued signals." *IEEE Transactions on Circuits and Systems I: Regular Papers* 56.12 (2009): 2634-2643.

[37] Garrido, Mario, et al. "Pipelined radix-2^k feedforward FFT architectures." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 21.1 (2013): 23-32.

[38] Pekurovsky, D. (2012). P3DFFT: A framework for parallel computations of Fourier transforms in three dimensions. *SIAM Journal on Scientific Computing*, *34*(4), C192-C209.